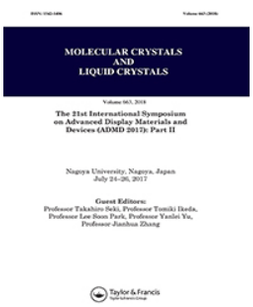

Molecular Crystals and Liquid Crystals

ISSN: 1542-1406 (Print) 1563-5287 (Online) Journal homepage: http://www.tandfonline.com/loi/gmcl20

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To cite this article: Joon-Yub Kim, Yeon Tae Jeong, Choon-Sang Park, Heung-Sik Tae & Byung-Gwon Cho (2018) Study on overlap scan waveform for low write voltage in AC plasma display panel, Molecular Crystals and Liquid Crystals, 663:1, 124-131, DOI: 10.1080/15421406.2018.1470600

To link to this article: https://doi.org/10.1080/15421406.2018.1470600

Published online: 04 Jun 2018.

MOLECULAR CRYSTALS AND LIQUID CRYSTALS
2018, VOL. 663, 124–131
https://doi.org/10.1080/15421406.2018.1470600

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Study on overlap scan waveform for low write voltage in AC plasma display panel

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ABSTRACT

Discharge characteristics in overlap scan waveforms are studied for lowering the write voltage in AC type plasma displays panel. The write discharge during the write period of the AC PDP occurs when negative pulses are applied to several hundreds of scan lines in time and a positive pulse is selectively applied to the write electrode. As the scan and write pulse widths during the write period are determined by the delay time of the write discharge, a high write voltage is typically used to stably generate the discharge within the pulse width. However, a high write voltage induces the high power consumption and causes the low efficiency of the AC PDP. Meanwhile, when the applied write voltage is decreased for the low power consumption, the discharge delay time will surely increase. If the pulse width of the scan electrode is increased so that the discharge occurs within the pulse width, the wall charge will be stably accumulated in a cell. Therefore, the widths of the write pulses are equal to the conventional time to make the same total write time, and overlapped waveforms in the scan lines are proposed by extending only the widths of the scanning pulses. Even if a low write voltage is applied, the discharge delay time will naturally be delayed, but the write discharge stably is occurred within the pulse width due to the long width of the scan pulse.

KEYWORDS

Discharge characteristic; discharge time; low write voltage; overlap scan; plasma display

1. Introduction

The AC type plasma display panel (AC PDP) was once a promising device as a large display device, but it has not been produced because of some problems such as high power consumption [1, 2]. However, if some problems are solved, it is expected to be a very attractive device as a large display. There are two kinds of power consumption generated from AC PDP, one is the effective power generated by the discharge and the other is the reactive power generated by the external applied voltage [3]. Since the effective power consumption related to the intensity of the light by the discharge is not controllable, the reactive power consumption should be lowered to reduce the total power consumption. The driving waveform of the AC PDP is roughly divided into three periods – reset, write, and sustain periods [4]. Since the waveform does

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not change rapidly during the reset period, the power consumption is small. In the sustain period, the power consumption is very high in the sustain period because the square waveforms of several hundred voltage are alternately applied to the two upper electrodes. But the technology of the energy recovery circuit could reduce the power consumption [5]. On the other hand, as hundreds of scan and write pulses are applied during the write period, it is very difficult to use an energy recovery circuit [6]. Therefore, the scan and write voltages must be lowered in order to lower the power consumption during the write period [7]. Among them, the method of lowering the write voltage is most effective because the scan voltage does not greatly affect the power consumption. Another reason for lowering the write voltage is that if the breakdown voltage of several driver IC components connected to the write electrode is lowered, the durability can be improved by relieving the stress transmitted to the component. In addition, the maximum voltage that can be tolerated by the write driver IC component can also be lowered, which is a great help in lowering the part price [8].

When a write pulse is applied to the vertical line while the scan pulses are applied at constant intervals according to time from the beginning to the end of the horizontal line during the write period, a write discharge is produced in the cells that meet each other. If this write discharge is stably produced within the width of the scan and write pulses, the light is normally generated during the sustain period. However, if the write voltage is lowered, the write discharge may be unstable or the discharge may fail to generate light in the sustain period.

When a voltage is applied to the plasma display panel, a discharge delay phenomenon necessarily occurs. The stable accumulation of the wall charge is performed only when a write discharge should generated within the width of the scan and write pulses during the write period, and the normal light is generated by stable discharge during the sustain period. The delay time of the write discharge can be shorter as the write voltage is higher, but causes an adverse effect that the power consumption is increased. Therefore, if the write voltage can be lowered while stably generating the write discharge, the power consumption of the AC PDP can be lowered.

In this study, the overlap scan waveform is proposed to generate discharge stably even if the write voltage is decreased to low the power consumption. The overlap scan waveform is a waveform in which the widths of the write pulses remain unchanged and the widths of the scan pulses are increased to overlap each other. That is, the waveform is designed to overlap the next scan pulse by increasing the width of one scan pulse. First, when the conventional driving waveform is applied, the maximum and minimum voltages of the write pulses according to the scan time are measured and the respective delay times of write discharge are measured. The maximum and minimum voltages of the write voltage are also measured when the overlap scan waveform is applied and compared with the conventional method.

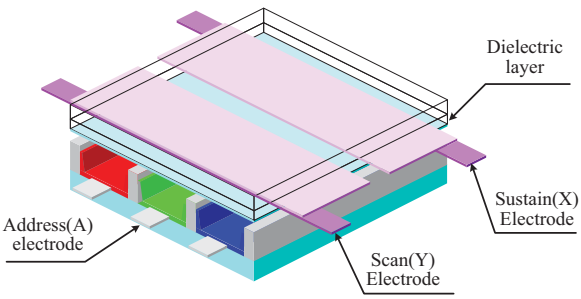


Figure 1. Structure of AC PDP used in experiment.

Table 1. Specification of AC PDP used in experiment.

Upper plate	Bus electrode width	110 μm
	ITO width	360 μm
	ITO gap	85 μm
Lower plate	Write electrode width	150 μm
	Barrier rib height	120 μm
	Barrier rib width	60 μm
Gas mixture	Ne (93%) – Xe (7%)	

2. Panel and driving waveform

Figure 1 shows the structure of an AC PDP with three cells used in the experiment, and Table 1 shows the specifications of the panel. There are two electrodes on the upper plate, separated by the sustain (X) and scan (Y) electrodes. These electrodes are also called a bus electrode. ITO, which is a transparent electrode, is deposited on the central portion of each bus electrodes. Since the transparent ITO electrode does not block the light generated in the cell, there is an advantage that the electrodes can be designed close to each other so that the discharge can easily occur between the two electrodes of the upper plate. The dielectric layer on the upper plate which is in contact with the discharge space lastly protects the electrodes without directly exposing it. In the lower plate, the write electrodes W are arranged in a direction perpendicular to the two electrodes of the upper plate, and are separated into barrier ribs each other. It is coated with Red, Green, and Blue phosphors, which are the three primary colors of light, on the write electrode. The gas used in the cell was a Ne-Xe mixed gas, as shown in Table 1.

Figure 2 shows a conventional driving waveform applied to three electrodes during one sub-frame time used in the experiment. The AC PDP represents the luminance by a combination of gradations divided into a plurality of sub-frames during one TV frame time, and the sub-frames are divided into reset, write and sustain periods, respectively. The reset period serves to make the wall charges accumulated in the entire cell for the same state and rearrange the wall charges to generate the address discharge. In the write period, when the scan waveforms are sequentially applied to the Y electrode while a constant voltage is applied to the X electrode and the pulses are selectively applied to the A electrode, the write discharge

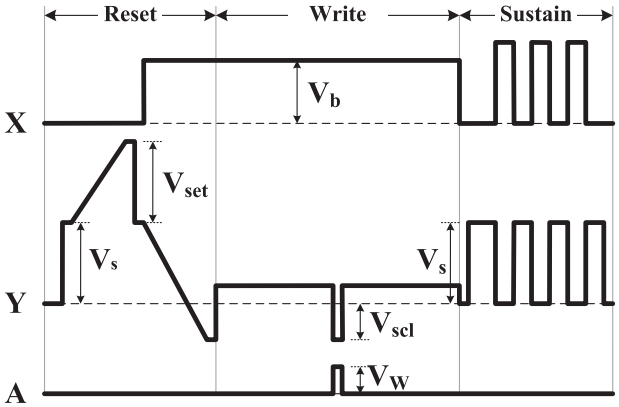
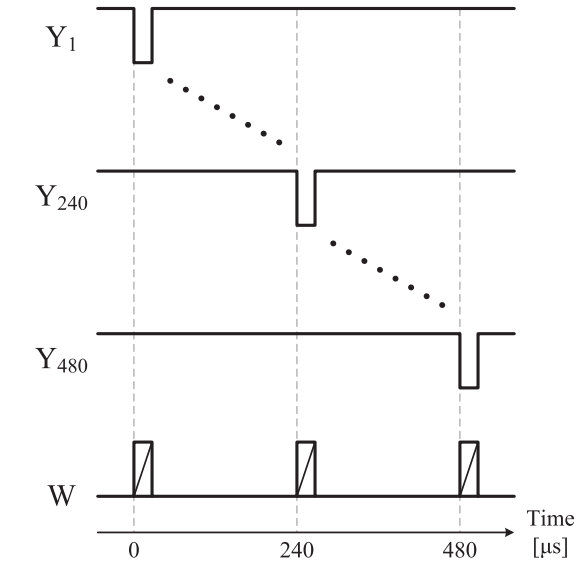
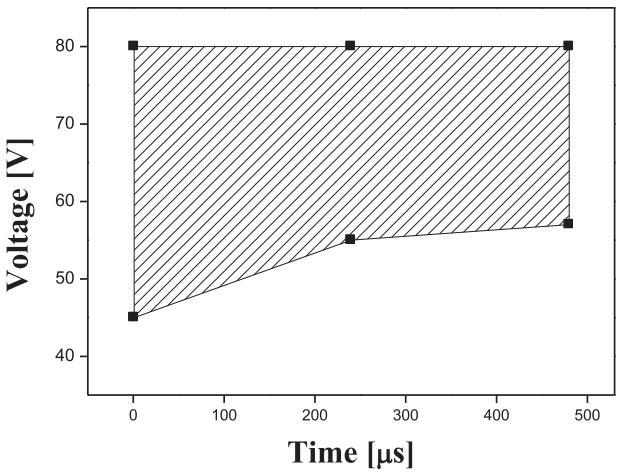


Figure 2. Conventional driving waveform during one sub-frame time.



(a)



(b)

Figure 3. Driving waveform applied to Y electrodes in write period over time (a) and margin of write voltage (b).

is produced only in the selected cell. When the write discharge occurs, wall charges are accumulated inside the cell, and light is generated by a square waveform alternately applied to the X and Y electrodes during the sustain period.

3. Experiment

Figure 3(a) shows each scan and write waveform when the width of one scan pulse is 1 μs in the Y electrode with 480 horizontal lines during the write period. Y_1 is at the first scan line,

Y_{240} is at the middle line, and Y_{480} is the scan waveform at the last line. The driving waveforms at other times are omitted. The write voltage was applied so as to have the same width at the same time as the scan waveform of the scan electrode. The diagonal line in the write pulse means that it is selectively applied.

Figure 3(b) shows the margin of the write voltage when the write pulse is applied to each position in Fig. 3(a). In the plasma display panel, a voltage margin indicates the region in which a discharge occurs successfully without failure. That is, in Fig. 3(b), it means that the discharge is failed or the misfiring discharge occurs outside of the line. By the way, the reason why the maximum voltage is 80 V in the figure is because it is the maximum voltage that the IC can withstand in the write circuit, and is not actually used due to the low power consumption by the high write voltage. The minimum voltage that can generate a discharge is the lowest on the first line, and high on the middle and last lines. The reason for the lowest write voltage in the first line is that many priming particles and wall charges generated during the reset period in Fig. 2 and have a large effect on the first discharge. The results in Fig. 3 show that the write voltage should be at least 60 V in order to produce the discharge stably by the conventional driving waveform under the condition of the panel used in the experiment.

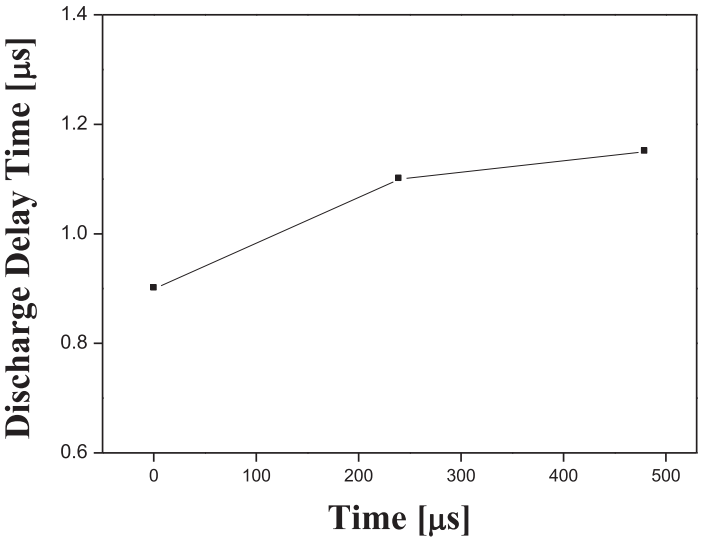
Figure 4(a) shows the delay time of the discharge according to the time change during the write period when the write pulse width is 1 μs and the voltage is 60 V, and Fig. 4(b) shows the optical waveform with time when the scan and write pulses are applied. It is confirmed that the write discharge is delayed over time when the voltage is fixed at 60 V in the write voltage margin of Fig. 3(b). The size of the discharge also weakened over time and the distribution of the discharge became wider. On the other hand, there was no significant difference in the intensity of the discharge in the middle and the last time.

4. Overlap scan waveform

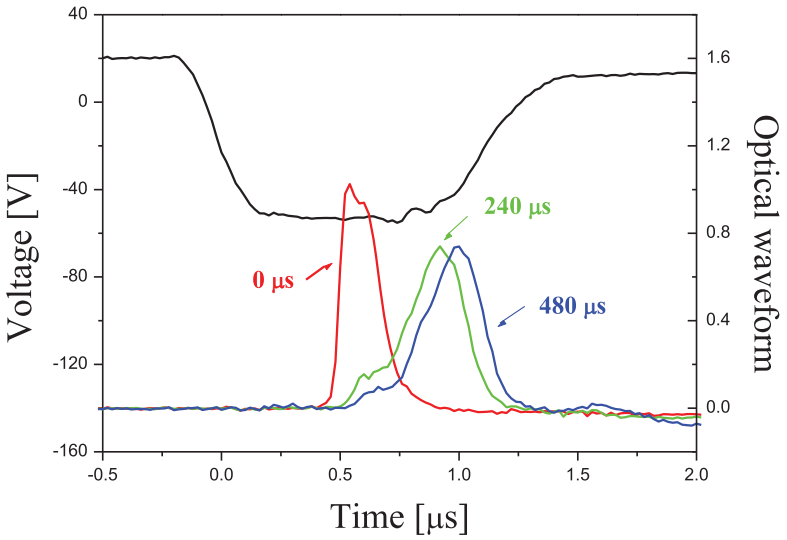
In this study, the overlap scan waveform is applied to accumulate the wall charge in the cell stably and generate the sustain discharge normally even if the discharge is delayed by the low write voltage rather than shortening the discharge delay time. In other words, the write discharge is inevitably delayed when a low write voltage is used to lower the power consumption, and the overlap scan waveform is a waveform that the discharge can be stably generated by extending the pulse width by a predetermined time at each scan electrode. However, in order to keep the total write time constant, in the proposed overlap scan waveform, the application time of the pulses in each scan line was overlapped by the increased amount, and the write pulse is applied with the same pulse width as the conventional one.

Figure 5(a) shows the overlap scan waveform applied to the Y electrodes and the write pulse on the W electrode during the write period. Among the three scan waveforms, the reason why the write pulse is applied only to the middle waveform in the W electrode is to investigate whether or not the production of the misfiring discharge due to the overlapped time in the preceding scan waveform. That is, it is normal that a discharge should be generated by the pulses of the Y_n and W electrodes, but there is a possibility that misfiring discharge may occur by the overlapped pulse width (Δt) at the Y_{n-1} electrode. Also, the pulse on the Y_{n+1} electrode is for measuring whether or not there is an effect by the discharge on the previous scan electrode. S_1 and S_2 are logic signals of the scan IC for overlapping the scan waveforms. The waveform can be overlapped by dividing the logic signals into odd and even signals.

Figure 5(b) shows the voltage margin at three positions according to the overlap time (Δt) when the driving waveform of Fig. 5(a) is applied. In the first time (first), since there was no previous scan pulse, it was measured at the second scan time to measure whether there



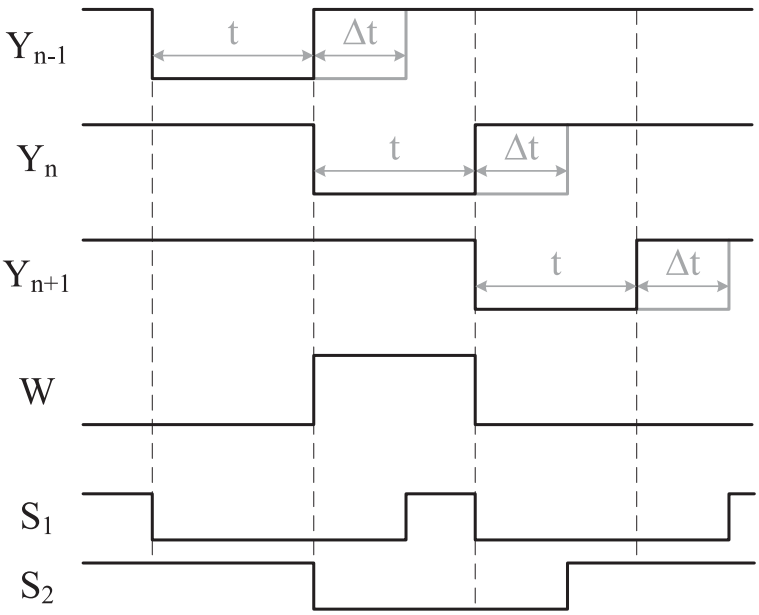
(a)



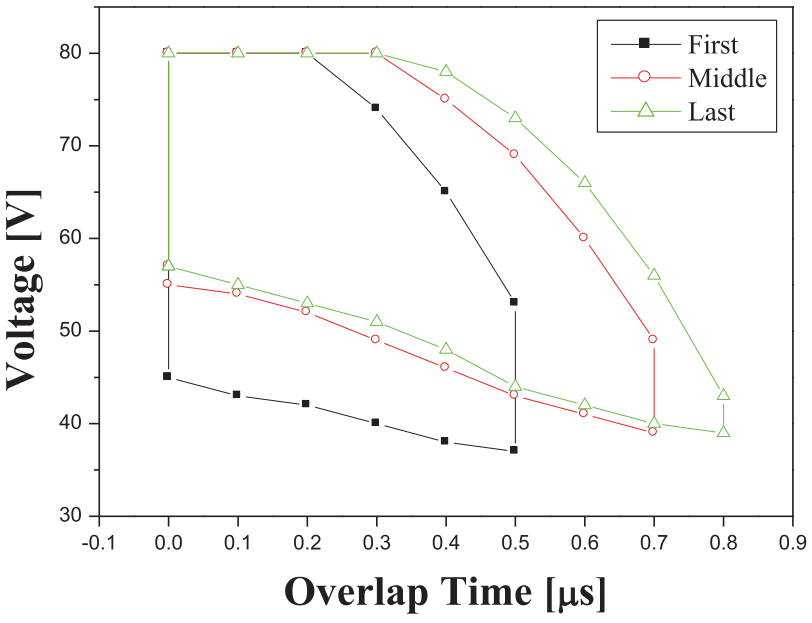
(b)

Figure 4. Delay of the discharge time with changes in time during write period (a) and optical waveforms with time when the scan and write pulses is applied (b).

was a misfiring discharge with the adjacent line. Compared with other experimental results in Fig. 5(b), the reason why the maximum voltage drops sharply as the overlap time increases at the first time is because the misfiring discharge occurs at the time of overlapping with the pulse at the previous electrode by the occurrence of the fast write discharge. Namely, since the time Δt at the Y_1 electrode overlaps the time t at the W electrode, the misfiring discharge has occurred. If the write voltage is lowered, the discharge is delayed and the misfiring discharge can be reduced. In addition, it can be seen that the voltage is slightly lowered by the overlap time. As the overlap time increased, the discharge delay time was longer but the production of



(a)



(b)

Figure 5. Overlap scan waveform applied to the scan electrodes and a write pulse during write period (a), a voltage margin in three positions with overlap time.

the discharge was successful even at low voltage. Though the measured results of the middle and last time tended to be similar to those of the first time, it could be seen that the misfiring discharge was not generated and the write discharge was successfully produced even when the overlap time was longer than the first time. The write voltage margin on the entire panel indicates the innermost area when the three measured margins are overlapped. While the voltage level at time 0 is the minimum write voltage in the conventional driving method, the overlap time from 0.1 to 0.8 μs time is the minimum write voltage in the proposed overlap driving method. At the overlap time of 0.5 μs, the minimum voltage could be lowered by about 13 V compared to the conventional driving method. Reducing the minimum write voltage will lower the cost of the data IC components used on the write electrode and will also contribute to lower power consumption depending on how many write pulses are used in the various patterns.

5. Conclusions

The overlap scan driving method was proposed to decrease the write voltage in which the width of the scan pulse is only increased under maintaining the width of the write pulse in the AC plasma display panel. First, the maximum and minimum write voltages were measured during the scan time when a write pulse width was 1 μs, and then the write discharge delay time was measured when the write voltage was fixed at 60 V. Due to the disappearance of priming particles and wall charge inside the cell, the write discharge delay time increased with time. Using the long discharge delay time, the waveforms of the scan electrodes were overlapped with each other so that the write discharge was stably generated. As a result, it is expected that the write voltage can be lowered by about 13 V compared with the conventional one, and it can be lowered by about 50 W by 42 inches.

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